

# Errata sheet

# IPC@CHIP SC145

#### Order No.:

IPC@CHIP SC145-0001:	571076
IPC@CHIP SC145-0002	571088

This document details the hardware/silicon errata known at the time of publication for the IPC@CHIP Embedded Controller SC145



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#### **Document Revision History** 1

Version	Date	Comments
1.00	01.06.2016	Initial version
2.00	07.12.2016	ETH0.1 Solution updated
		ICPU.1 Problem updated
		ICPU.2 Introduction updated
2.01	01.02.2017	SPI3.1 added
1		Order No. updated

#### 2 **Product identification**

The IPC@CHIP SC145 is marked with:

Type: SC145

Version: e.g. ES H01 (ES means Engineering Sample, H01 the HW Revision) (# is part of the MAC of eth0, e.g. 00:30:56:50:00:97)

Serial number: e.g. 0097

This errata sheet refer to

SC145 - ES H01 SC145 - H02



# 3 **Product errata**

### 3.1 ETH0.1 – Sporadically communication problems

#### Introduction:

A built-in 10/100Mbit/s PHY (eth0) is on board, the TPI Network is to realize on the associated board. Depending on the TPI Network Circuit and used switches two different errors may occur:

#### Problem A:

Sporadically the communication shows in different way corrupted packets. The establishing of communication (first link phase) decides for error case or proper working. The established behaviour (ok or faulty) seems long term stable. The communication establishing at Power on, reboot or disconnect/connect ETH leads to same behaviour.

#### Work-around:

Use a different switch, or disconnect/connect ETH0 until the problem is gone.

#### Problem B:

If the SC145 device is turned-off (no power) the connected Ethernet switch will detect a 10 MBit link after about 30-40 seconds. After this link was detected by the connected Ethernet switch, the connected Ethernet switch does no longer work correctly. It seems that a lot of Ethernet packets are dropped now. This problem is detected with a couple of Gigabit Ethernet Switches, e.g. Netgear ProSafe GS108, Netgear ProSafe GS108P or AVM Fritzbox 7490.

#### Work-around:

Use a different switch, or disconnect ETH0 during the SC145 Board is not powered.

#### Proposed Solution

To be fixed in the next HW Revision.

### Solution Fixed in revision H02

# 3.2 ICPU.1 – Internal processor Qualification Level & Silicon Revision

#### Introduction:

The populated i.MX 6UltraLite processor on IPC@CHIP SC145 has two version descriptions: Qualification Level / Silicon Revision



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#### Problem:

The populated processor is

H01: Qualification Level: PC - Prototype Samples / Silicon Revision: A 1.0

H02: Qualification Level: MC – Mass Production / Silicon Revision: A 1.1.

The Versions have the ICPU.x errata's.

#### Work-around:

Refer to according sub item.

#### Proposed Solution

No fix scheduled

# 3.3 ICPU.2 – I2C clock speed 400 kHz, the SCL period violates the I2C specification

#### Introduction:

The described I2C errata are owned by processors with Revision:

Silicon Revision: A 1.0 Silicon Revision: A 1.1

#### Problem:

If he I2C is programmed to operate at the maximum clock speed of 400 kHz (as defined by the I2C spec), the SCL clock low period violates the I2C spec of 1.3 µs min.

Work-around: Configure the I2C frequency to max. 375 kHz

Proposed Solution No fix scheduled.

# 3.4 SPI3.1 – Documentations for Pin Configuration

Introduction:

The Pin Configuration is described in Graphic illustrations, tables and ECAD Services.

#### Problem:

The MOSI3 and MISO3 are swapped in the documentation.

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Work-around:

Refer the "SC1x5 Hardware manual" with correct tables and figures.

Proposed Solution

No fix scheduled.